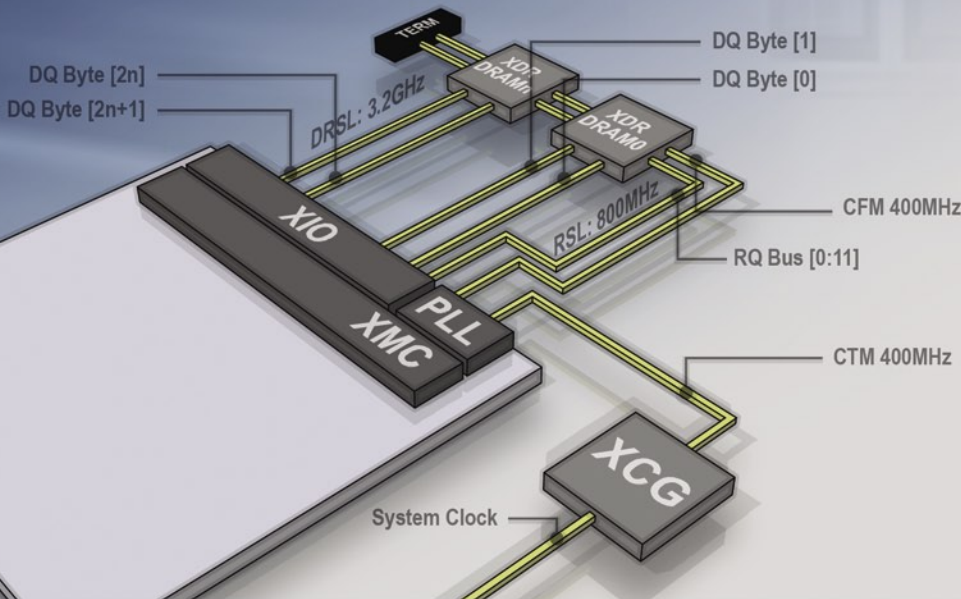


# Rambus®

## XDR™

### Memory Controller Interface Brief

XDR DRAM System Example



#### APPLICATIONS

- Consumer Electronics
- Computer Graphics
- Server Main Memory
- Networking
- Supercomputing

#### BENEFITS

- Highest bandwidth for demanding applications
- Fast time-to-market
- Simplified system design and test with FlexPhase™
- Minimized risk from fully validated designs
- Scalable with Dynamic Point-to-Point technology
- System engineering services for reduced time-to-market
- XDIMM module support for high capacity applications

## High Performance Memory Interface Solution

### XDR DRAM: Delivers a Quantum Leap in Memory Bandwidth

The Rambus XDR DRAM achieves an order of magnitude increase in DRAM bandwidth over today's best-of-class memory systems. The XDR Interface uses a small number of very high-speed signals to carry all address, data, and control information.

XDR architecture provides a total system solution to many of the complex issues and problems that engineers face in designing cost effective, high-performance memory subsystems.

### XDR Solution: Highest Bandwidth, Lowest Chip Count

XDR memory interfaces can deliver upwards of 250GB/s of total bandwidth for demanding systems. Any number of interfaces may be integrated into the controller chip to supply the specified memory bandwidth. The XDR solution was engineered to be effective in small footprint, high-bandwidth consumer systems as well as in high-performance main memory applications.

### A Solution for High Bandwidth Applications

The XDR interface technology is implemented on CMOS controller chips for applications such as high-performance main memory, PC graphics, game consoles, advanced digital consumer systems, high-performance networking systems, and other demanding applications requiring high bandwidth memory subsystems. XDR DRAM delivers the complete system solution for memory bandwidth intensive applications.

### Highest Bandwidth per Device

The Rambus XDR memory interface achieves an order of magnitude higher performance than today's memories while utilizing the fewest ICs. For example, a single, 2-byte wide, 3.2 GHz XDR DRAM component provides up to 6.4 GB/sec bandwidth over the XDR Interconnect. The XDR roadmap supports a performance path up to 8GHz data rates delivering up to 16 Gigabytes / second per DRAM.

### XDR System Controller Chip

The XDR memory solution was developed to support a broad range of applications and component implementations spanning multiple semiconductor and DRAM technology generations. XDR system controller chips consist of an XDR IO cell and an XDR memory.

### XDR Memory Controller

The XMC is a configurable soft macro reference design provided by Rambus. Customers may integrate the XMC directly or use it as a reference design in developing and verifying their own memory controller.

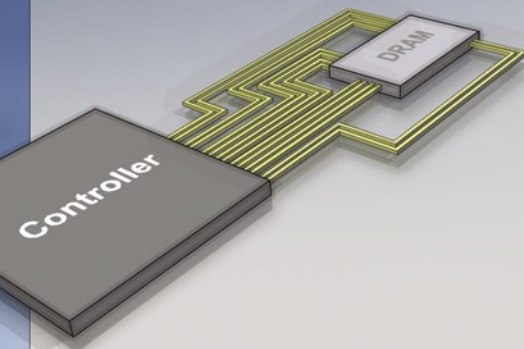
XDR reference memory controllers from Rambus or other providers offer flexibility to accommodate a wide variety of expected DRAM configurations and can be optimized to support customer specific environments.

## XDR Interface Cell Building Blocks

FLEXPHASE™ SIMPLIFIES PCB DESIGN BY ELIMINATING DATA TRACE LENGTH MATCHING

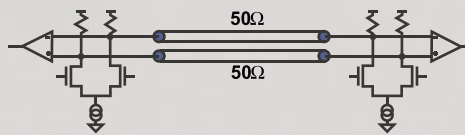
3.2GHZ BI-DIRECTIONAL DIFFERENTIAL SIGNALING (DRSL)

OCTAL DATA RATE SIGNALING (ODR)



XDR PHYSICAL SIGNALING SYSTEM

ODR IS 8 BITS PER CLOCK



## FEATURES

### Highest pin bandwidth

- 3.2 to 8.0 GHz data rate
- Octal Data Rate (ODR) signaling
- Bi-directional differential RSL (DRSL)
- Programmable on-chip termination
- Adaptive impedance matching
- Dynamic Point-to-Point scalability

### Low power

- 1.8V Vdd
- Programmable ultra-low-voltage I/O signaling
- Power-down self-refresh support
- Dynamic data width support
- Per pin I/O power-down

### Ease in system design

- Data line length mismatch
- Compensation with FlexPhase™
- Minimum pin count
- Automated system characterization and margining

## XDR IO Cell

The XIO cell resides on the ASIC controller, and consists of a collection of hard and soft macros, which provide the physical layer interface between the memory controller and the XDR Interconnect. The XIO cell blocks are flexible to embrace differing layout concerns.

XDR hard macros are available in a variety of foundry sources across multiple process technology generations.

## XDR Interface Signaling

XDR solutions use the best of both worlds, Differential Rambus Signaling Levels (DRSL) for scalable high speed point to point bi-directional data signals and Rambus Signaling Levels (RSL) for source synchronous bussed address and command signals to multiple DRAM devices. The point to point bus allows multi-GHz speeds, while the bussed address allows scalable capacity of up to 36 DRAM devices per request bus block.

The combination of DRSL and RSL signaling provides a high-performance interconnect for the most demanding of applications. Ultra-low-voltage-swing-differential signals minimize di/dt, thereby:

- Reducing ground bounce
- Decreasing power consumption
- Reducing electromagnetic interference
- Increasing scalability to higher data rates
- Improved noise immunity via common mode rejection

## Octal Data Rate Transfers

Octal Data Rate transfers are used between the XDR ASIC controller and the XDR DRAM. Eight bits of data per clock are transferred per 400MHz clock cycle effectively delivering data at 3.2GHz data rates. The XDR DRAM data rates are scalable to 8.0 GHz as bandwidth needs increase.

## FlexPhase - Easy System Design & Lower Cost

FlexPhase circuits are contained in the ASIC's XIO cell. They skew individual data bit output timing from the ASIC to the XDR DRAM to present a synchronized parallel data word to the XDR DRAM. Controller XDR FlexPhase I/O circuits also compensate for systematic timing errors with a resolution finer than 2.5ps.

FlexPhase circuits are also used to account for each bit's individual skew from the XDR DRAM to the ASIC.

## XDR Interface: The Complete System Solution

The XDR memory architecture was designed as a complete system solution. This product family solves the many problems facing design engineers developing cost-effective, high-performance memory subsystems.

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